

# **CIRCUIT SUBSTRATE AND FABRICATION METHOD THEREOF**

## **BACKGROUND OF THE INVENTION**

### **Field of Invention**

[0001] This invention relates to a circuit substrate and a fabrication method thereof.

5 More particularly, the present invention is directed to a circuit substrate, suitable for an integrated circuit, and fabrication method thereof.

### **Related Art**

[0002] Presently, circuit substrate is commonly employed as carrier in electrical industry. Not only circuit substrate is employed as printed circuit board (PCB) but  
10 also package substrate, which is applicable to an integrated circuit package. Recently, a high-density circuit substrate having multiple layers and conductive traces with fine pitches is improved for the integration of the integrated circuits (ICs), and the need of thinner ICs package and higher input/output counts.

[0003] As shown in FIG. 1, a circuit substrate 10 mainly includes a board 100. The  
15 board 100 comprises a core board 101, a plurality of insulating layers 110 and conductive traces layers 130. The insulating layers 110 and the conductive traces layers 130 are interlaced with each other. The conductive traces layers 130 are electrically connected with each other through vias 140 such as through holes, buried vias or blind vias. Now taken a through hole for example as shown in FIG. 1, initially,  
20 the insulating layers 110 and the conductive traces layers 130, which are interlaced with each other, are penetrated to form a through hole therein by the method of mechanical drilling or laser ablation. Next, the inner wall of the through hole is electro-less plated with a copper film and then another copper layer is deposited on the copper film. Finally, the through hole is filled with an insulating material, for

example epoxy and ink. Now referring to FIG. 2, via land 160 is disposed at the periphery of the via 140 to electrically connect the conductive traces 130a and the via 140. Generally speaking, if the diameter of the via 140 is about 300 $\mu$ m, the diameter of the via land 160 will be about 500 $\mu$ m. In addition, a landless design can be employed to save the area for the arrangement of the via land 160. However, the process of the landless design is complex and the cost is increased.

[0004] As shown in FIG. 2, the via lands 160 occupy a lot of areas so that the areas for laying out the conductive traces are reduced. In such a manner, the conductive traces 130a will be finer and the pitches between the conductive traces will be fined down. Consequently, it will be difficult to fabricate the circuit substrate. Besides, the quality of the electricity will be seriously affected in that, with reference to FIG. 2, the bent portions of the conductive traces and the distance of the signal transmission are increased.

[0005] As shown in FIG. 3, the previously mentioned problems can be solved and improved by directly reducing the diameter of via 240. Plasma, Nd:YAG laser and excimer laser can be utilized to form via 240 with smaller diameter. When the diameter of the via 240 is reduced, the areas for laying out the conductive traces 230a can be increased to reduce the bent portions of the conductive traces 230a. However, the fabrication method of plating metal layer on the inner wall of the via 240 will become more complex due to the smaller diameter of the via 240.

## SUMMARY OF THE INVENTION

[0006] In view of the above-mentioned problems, an objective of this invention is to provide a circuit substrate and a fabrication method thereof, which can increase the density of the conductive traces layout in the circuit substrate without reducing the width of the conductive traces and the pitches between the conductive traces.

[0007] It is another objective of the invention to provide a circuit substrate and a fabrication method thereof, which can reduce the distance of signal transmission.

[0008] To achieve the above-mentioned objective, a circuit substrate of this invention includes a board, a plurality of metal layers and an insulator. In this invention, the board includes a plurality of conductive traces layers and insulating layers, and at least one via formed therein. The metal layers are formed on the inner wall of the via and electrically connected to the corresponding conductive traces layers. The via is filled with an insulator so that the metal layers disposed in the same via are electrically isolated from each other.

[0009] Furthermore, the invention also discloses a fabrication method of the circuit substrate as mentioned above. The fabrication method includes the steps of providing a board with a plurality of conductive traces layers and insulating layers wherein at least one via is formed in the board, forming metal layers on the inner wall of the via, cutting the via to form at least one cutting street to separate the metal layers into a plurality of separated metal layers and filling an insulator in the via and the cutting street.

[0010] Circuit substrate of this invention is formed by filling an insulator in the via and the cutting street so that the metal layer formed on the inner wall of the via is separated into a plurality of separated metal layers. In such a manner, the separated metal layers in the via are electrically isolated from each other. In other words, each separated metal layers in the same via can be provided to electrically connect its corresponding conductive traces layer. Consequently, the number of the vias will be reduced so as to increase the density of the conductive traces layout. Besides, it can also reduce the bent portions of the conductive traces so as to reduce the distance of signal transmission.

[0011] Moreover, this invention further discloses a fabrication method of the circuit substrate as mentioned above. The method includes the steps of forming a metal layer on the inner wall of the via, cutting the via to form at least one cutting street to separate the metal layer into a plurality of separated metal layers. In such a manner, the via can be separated into a plurality of separated vias. Consequently, not only this process can simplify the process of plating metal layers on the inner wall of smaller via, but also speed up the formation for large amount of the vias.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0012] The invention will become more fully understood from the detailed description given herein below illustrations only, and thus are not limitative of the present invention, and wherein:

- [0013] FIG. 1 is a cross-sectional view of a conventional circuit substrate;
- [0014] FIG. 2 is a top view of the conventional circuit substrate of FIG. 1;
- [0015] FIG. 3 is a top view of another conventional circuit substrate;
- [0016] FIG. 4A is a top view of a circuit substrate in accordance with the present invention;
- [0017] FIG. 4B is a cross-sectional view of the circuit substrate of FIG. 4A;
- [0018] FIG. 5A to 5H are cross-sectional views illustrating the process flow of a fabrication method of the circuit substrate of FIG. 4A; and
- [0019] FIG. 5I to 5J are top views illustrating the process flow of a fabrication method of the circuit substrate of FIG. 4A.

### **DETAILED DESCRIPTION OF THE INVENTION**

[0020] The circuit substrate and fabrication method thereof according to the

preferred embodiment of this invention will be described herein below with reference to the accompanying drawings, wherein the same reference numbers refer to the same elements.

[0021] In accordance with a preferred embodiment as shown in FIG. 4A and 4B, a  
5 circuit substrate 40 includes a board 400, a via 440, metal layers 450a and 450b, and  
an insulator 480. The board 400 comprises a core board 401, and a plurality of  
insulating layers 410 and conductive traces layers 430 wherein the insulating layers  
410 and the conductive traces layers 430 are interlaced with each other. The material  
of the insulating layers 410 can be Bismaleimide-Triazine (BT), glass epoxy resins  
10 (FR4), epoxy or polyimide. The conductive traces layer 430 can be formed by the  
steps of forming a copper foil on the surface of the insulating layer 401, forming a  
patterned photo-resist layer on the copper foil, removing a portion of the copper foil  
by etching and using photo-resist layer as a mask, and removing the photo-resist layer.

[0022] Via 440 can be formed by a mechanical method or a chemical method, and  
15 the via 440 can be a through hole, a buried via or a blind via. Metal layers 450a and  
450b can be formed on the inner wall 442 of the via 440 by the method of electro-less  
plating or direct plating. Via lands 460a and 460b are disposed on the board 400 and  
at the periphery of the via 440, and the material of the via lands 460a and 460b are  
with good electrical conductivity. Generally speaking, the material of the via lands  
20 460a and 460b is substantially the same as the conductive traces 430a and 430b, for  
example copper metal. The via 440 is filled with an insulator 480 which separates the  
via 440 into a plurality of separated vias (not shown), and the metal layers 450a and  
450b are electrically isolated from each other by the insulator 480. In addition, the via  
lands 460a and 460b are also electrically isolated from each other. The insulator 480  
25 can be made of insulating materials, for example epoxy resin and ink. Besides, the

metal layers 430a and 430b are electrically connected with the conductive traces 430a and 430b through the via lands 460a and 460b.

[0023] FIG. 5A to FIG. 5G illustrate the fabrication method of the circuit substrate in accordance with the invention as mentioned above. As shown in FIG. 5A, a core board 401 that is made of a prepreg with higher hardness and higher glass transition temperature ( $T_g$ ) is provided with a copper foil 420 disposed on the top surface 401a and bottom surface 401b. Referring to FIG. 5B and FIG. 5C, the conductive traces layer 430 as shown in FIG. 5C are formed by the steps of forming photo-resists 421 on the copper foils 420 and patterning the copper foils 420 by exposure, development and etching processes.

[0024] Next, an insulating material is coated on the conductive traces layers 430 to form insulating layers 410 as shown in FIG. 5D. Then the steps as shown in FIG 5A., FIG. 5B and FIG. 5C are repeated to form the board having a plurality of insulating layers 410 and a plurality of conductive traces layers 430 wherein the insulating layers 410 and the conductive traces layers 430 are interlaced which each other. After that, as shown in FIG. 5E, the via 440 is formed by the methods of mechanical drilling, laser ablation, photochemical reaction and plasma etching.

[0025] Referring to FIG. 5F, a metal layer 450 is formed on the inner wall 442 of the via 440 and the surfaces 412 and 414 of the insulating layers 410. Since the inner wall 442 of the via 440 and the surfaces 412 and 414 of the insulating layers 410 are made of composite material, the activated material, for example barium (Ba) and conductive polymer, shall be disposed on the inner wall 442 of the via 440 and the surfaces 412 and 414 of the insulating layers 410 in advance. Then, a thin copper film is formed on the inner wall 442 of the via 440 and the surfaces 412 and 414 of the insulating layers 410 by the method of electro-less plating, wherein the thickness of

the thin copper film is about  $0.5\ \mu\text{m}$ . Next, another copper layer is directly formed on the thin copper film to form a metal layer 450, wherein the thickness of the metal layer 450 is about  $20\ \mu\text{m}$ . Besides, the metal layer 450 can be formed by the method of direct plating. The method of direct plating comprises the steps of forming a  
5 conductive polymer or a conductive carbon layer on the inner wall 442 of the via 440 and the surfaces 412 and 414 of the insulating layers 410, and forming the metal layer 450 on the conductive polymer or conductive carbon layer.

[0026] Referring now to FIG. 5G, a photolithography process is provided to form the conductive traces layers 430 and via lands 460 as shown in FIG. 5H. The  
10 photolithography process comprises the steps of forming photo-resist layers 451 on the metal layers 450 disposed respectively on the insulating layers 410, patterning the photo-resist layers 451 by exposure and development, etching a portion of the metal layers 450 by using the photo-resist layers 451 as a mask and removing the photo-resist layers 451.

15 [0027] Next, referring to FIG. 5I, the cutting street 470 of the via 440 is formed by cutting the via through the method of laser ablation wherein the methods comprise  $\text{CO}_2$  Laser, Nd:YAG laser and excimer laser. Besides, the cutting street 470 can be formed by the method of mechanical drilling, photochemical reaction or plasma etching. The cutting street 470 separates the via 440 into two separated vias (not  
20 shown). Consequently, the metal layer 450 of the inner wall 442 of the via 440 are separated into two separated metal layers 450a and 450b, and the via land 460 are also separated into two separated via lands 460a and 460b.

[0028] As shown in FIG. 5J, the via 440 is entirely filled with an insulator 480, for example epoxy resin. In such manner, the separated metal layers 450a and 450b  
25 disposed on the inner wall 442 of the via 440 can be electrically isolated from each

other and electrically connected to the conductive traces 430a and 430b respectively.

[0029] As mentioned above, this invention has following advantages.

1. The circuit substrate in accordance with this invention utilizes the insulator to separate the metal layer formed on the inner wall of the via into a plurality of separated metal layers which are electrically isolated from each other. Consequently, each metal layer can be electrically connected to different conductive trace. In other words, because the functions of a plurality of vias in a conventional circuit substrate can be integrated in one via as specified in this invention, the areas occupied by the vias can be reduced and the density of the conductive traces layout can be increased. Besides, the bent portions of the conductive traces will be reduced so as to shorten the distance of signal transmission.

2. The fabrication method in accordance with this invention comprises the steps of forming a metal layer on the inner wall of the via and cutting the via to form cutting streets to separate the metal layer into a plurality of separated metal layers. Consequently, this fabrication method not only prevents from the difficulty of plating process during the formation of the via with fine diameter but speeding up the formation for large amount of the vias.

[0030] Although the invention has been described in considerable detail with reference to certain preferred embodiments, it will be appreciated and understood that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims.